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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/781,879	02/20/2004	Ying-Hsin Li	LEE0031-US	4242

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EXAMINER	
HO, TU TU V	

ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 04/29/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

H·A

Office Action Summary	Application No.	Applicant(s)	
	10/781,879	LI ET AL.	
	Examiner	Art Unit	
	Tu-Tu Ho	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 February 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8 and 11-18* is/are rejected.

7)☒ Claim(s) *9,10,19 and 20* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *20 February 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Oath/Declaration

1. The oath/declaration filed on 08/11/2004 is acceptable.

Claim Objections

2. **Claims 18 and 19** are objected to because of the following informalities: Claims 18 and 19 each recites: "The diode of claim 16", however, it is apparent that the phrase should be "The diode of claim 17" because claim 16 already recites an intrinsic layer which together with the intrinsic region of claim 18 would require a new drawing; similarly, claim 19 as claimed would require a new drawing. For examination purposes, the dependency of each of claims 18 and 19 is based on claim 17.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in
> (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or
> (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. **Claims 1-3, 5, 11-13, and 15** are rejected under 35 U.S.C. 102(b) as being anticipated by Yamaguchi et al. U.S. Patent 6,118,154 (the '154 patent).

The '154 patent discloses in the figures, particularly Figures 4 and 5, and respective portions of the specification a diode a method of fabricating thereof as claimed.

Referring to **claims 1 and 11**, the reference discloses a diode a method of fabricating thereof, comprising:

a semiconductor layer, comprising:

a first region (39b, Fig. 5) of a first carrier concentration, wherein said first carrier concentration is of a first conductivity type (p);

a second region (39c) of a second carrier concentration, wherein said second carrier concentration is of a second conductivity type (n);

an insulator layer (11) disposed on said semiconductor layer, said insulator layer including at least a contact window (12); and

a metal layer (13 or 14) disposed on said insulator layer;

wherein said contact window exposes a portion of an upper surface of said semiconductor layer, said metal layer fills up said contact window to contact said semiconductor layer.

Referring to **claims 2 and 12**, the reference further discloses that said diode is formed by a thin-film transistor process (comparing Figs. 3 and 5; and wherein "thin-film transistor process" is interpreted broadly, i.e., a process for forming a thin-film transistor or a process for forming a transistor having a thin film), said diode is applied to a circuit (Fig. 4).

Referring to **claims 3 and 13**, the reference further discloses that said first region is adjacent to said second region ("adjacent" is interpreted broadly).

Referring to **claims 5 and 15**, the reference further discloses that said semiconductor layer further comprises a third region (39e) of a third carrier concentration, said third carrier concentration is of said first conductivity type (p), said third carrier concentration (p-) is smaller than said first carrier concentration (p+), said first region separates from said second region, said third region locates between said first region and said second region, said third region is adjacent to said first region.

4. **Claims 1-3 and 11-13** are rejected under 35 U.S.C. 102(b) as being anticipated by Finzi U.S. Patent 6,329,691 (the '691 patent).

The '691 patent discloses in Figures 3 and 4a, and respective portions of the specification a diode a method of fabricating thereof as claimed.

Referring to **claims 1 and 11**, the reference discloses a diode a method of fabricating thereof, comprising:

a semiconductor layer, comprising:

a first region (432) of a first carrier concentration, wherein said first carrier concentration is of a first conductivity type (p);

a second region (436) of a second carrier concentration, wherein said second carrier concentration is of a second conductivity type (n);

an insulator layer (no number) disposed on said semiconductor layer, said insulator layer including at least a contact window (directly above region 432, no number); and

a metal layer (no number) disposed on said insulator layer;

wherein said contact window exposes a portion of an upper surface of said semiconductor layer, said metal layer fills up said contact window to contact said semiconductor layer.

Referring to **claims 2 and 12**, the reference further discloses that said diode is formed by a thin-film transistor process (as evident from Fig. 4a), said diode is applied to a circuit (Fig. 3).

Referring to **claims 3 and 13**, the reference further discloses that said first region is adjacent to said second region.

Claim Rejections - 35 USC § 102 & 103

The following is a quotation of 35 U.S.C. §103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. **Claims 1-2, 4-5, 11-12, and 14-15** are rejected under 35 U.S.C. 102(b) as anticipated by or, in the alternative, under 35 U.S.C. 103(a) as obvious over Staab et al. U.S. Patent 5,610,790 (the '790 patent).

The '790 patent discloses in Figures 4 and 5, and respective portions of the specification a diode a method of fabricating thereof as claimed or substantially as claimed. Specifically, the reference discloses a diode a method of fabricating thereof without the claimed insulator layer and the contact window in the insulator layer.

More specifically and with reference to **claims 1 and 11**, the reference discloses a diode (500) a method of fabricating thereof, comprising:

a semiconductor layer, comprising:

a first region (502) of a first carrier concentration, wherein said first carrier concentration is of a first conductivity type (p);

a second region (503) of a second carrier concentration, wherein said second carrier concentration is of a second conductivity type (n);

However, as noted above, the reference fails to disclose an insulator layer disposed on said semiconductor layer, and further fails to disclose that said insulator layer includes at least a contact window and a metal layer disposed on said insulator layer and wherein said contact window exposes a portion of an upper surface of said semiconductor layer, said metal layer fills up said contact window to contact said semiconductor layer.

Nevertheless, as is known in the art, the '790 patent's diode structure 500 should inherently comprise an insulator of sorts to protect it from the environment, as is bone requiring skin for protection, and further inherently comprises electrical connections for the device to function, and the electrical connections should fill up a contact window etched in the insulator to contact said semiconductor layer (see, for example, Finzi U.S. Patent 6,329,691, Fig. 4a, cited above).

Therefore, the limitation is either: (1) inherent if one of ordinary skill in the art subscribes to the interpretation that the diode 500 inherently comprises the claimed insulator layer; or (2) obvious - if one yields to the argument that everything in a reference must be spelled out exactly word by word, element by element, to anticipate the claim - to one of ordinary skill in the art at the time the invention was made to modify because adding the insulator layer, and the necessary contact window and electrical metal contact, would help protect the diode 500 from the environment.

Referring to **claims 2 and 12**, the reference further discloses that said diode is formed by a thin-film transistor process (comparing Figs. 5 and 6; and wherein "thin-film transistor process" is interpreted broadly, i.e., a process for forming a thin-film transistor or a process for forming a transistor having a thin film), said diode is applied to a circuit (Fig. 4).

Referring to **claims 4 and 14**, the reference further discloses that said semiconductor layer further comprises a third region (504), said third region is intrinsic ("undoped", column 3, lines 25-31), said first region separates from said second region, said third region locates between said first region and said second region.

Referring to **claims 5 and 15**, the reference further discloses that said semiconductor layer further comprises a third region (504) of a third carrier concentration, said third carrier concentration is of said first conductivity type (p) (column 3, lines 25-31), said third carrier concentration (p-) is smaller than said first carrier concentration (p), said first region separates from said second region, said third region locates between said first region and said second region, said third region is adjacent to said first region.

6. **Claims 1-8 and 11-18** are rejected under 35 U.S.C. 102(e) as anticipated by or, in the alternative, under 35 U.S.C. 103(a) as obvious over Ker et al. U.S. Patent Application Publication 20040105203 (the '203 publication).

The '203 publication discloses in Figures 9 and 10, and respective portions of the specification a diode a method of fabricating thereof as claimed or substantially as claimed. Specifically, the reference discloses a diode a method of fabricating thereof without the claimed insulator layer and the contact window in the insulator layer.

More specifically and with reference to **claims 1 and 11**, the reference discloses a diode (D1) a method of fabricating thereof, comprising:

a semiconductor layer, comprising:

a first region (96b) of a first carrier concentration, wherein said first carrier concentration is of a first conductivity type (p);

a second region (96a) of a second carrier concentration, wherein said second carrier concentration is of a second conductivity type (n);

However, as noted above, the reference fails to disclose an insulator layer disposed on said semiconductor layer, and further fails to disclose that said insulator layer includes at least a contact window and a metal layer disposed on said insulator layer and wherein said contact window exposes a portion of an upper surface of said semiconductor layer, said metal layer fills up said contact window to contact said semiconductor layer.

Nevertheless, as is known in the art, the '203 publication's diode structure D1 should inherently comprise an insulator of sorts to protect it from the environment, as is bone requiring skin for protection, and further inherently comprises electrical connections for the device to function, and the electrical connections should fill up a contact window etched in the insulator to contact said semiconductor layer (see, for example, Finzi U.S. Patent 6,329,691, Fig. 4a, cited above).

Therefore, the limitation is either: (1) inherent if one of ordinary skill in the art subscribes to the interpretation that the diode D1 inherently comprises the claimed insulator layer; or (2) obvious - if one yields to the argument that everything in a reference must be spelled out exactly word by word, element by element, to anticipate the claim - to one of ordinary skill in the art at

the time the invention was made to modify because adding the insulator layer, and the necessary contact window and electrical metal contact, would help protect the diode D1 from the environment.

Referring to **claims 2 and 12**, the reference further discloses that said diode is formed by a thin-film transistor process (comparing Figs. 9 and 1; and wherein "thin-film transistor process" is interpreted broadly, i.e., a process for forming a thin-film transistor or a process for forming a transistor having a thin film), said diode is applied to a circuit (Fig. 10).

Referring to **claims 5 and 15**, the reference further discloses that said semiconductor layer further comprises a third region (98b) of a third carrier concentration, said third carrier concentration is of said first conductivity type (p), said third carrier concentration (p-) is smaller than said first carrier concentration (p+), said first region separates from said second region, said third region locates between said first region and said second region, said third region is adjacent to said first region.

Referring to **claims 7 and 17**, the reference further discloses a fourth region (98a) of a fourth carrier concentration, said fourth carrier concentration is of said second conductivity type (n), said fourth carrier concentration (n-) is smaller than said second carrier concentration (n+), said third region separates from said second region, said fourth region locates between said third region and said second region, said fourth region is adjacent to said second region.

Referring to **claims 4, 6, 8, 14, 16, and 18**, the '203 publication discloses a diode and a method of fabricating thereof substantially and as detailed above, and further discloses a third region as detailed above for claims 5 and 15, and a fourth region as detailed above for claims 7 and 17, but fails to disclose a third region or a fourth region or a fifth region, the third region or

the fourth region or the fifth region being intrinsic as claimed. However, the artisan, at the time the invention was made, would easily recognize, therefore would have been obvious, that a diode having an intrinsic region as claimed would increase the breakdown voltage, as is known in the art and as disclosed, for example, by Nemoto PGPUB-DOCUMENT-NUMBER: 20010015445, paragraph [0003].

Claim Rejections - 35 USC § 103

7. **Claims 3-4, 6, 13-14, 16, and 18** are rejected under 35 U.S.C. §103(a) as being unpatentable over Yamaguchi et al. U.S. Patent 6,118;154 (the '154 patent).

Referring to **claims 3 and 13**, the '154 patent discloses a diode a method of fabricating thereof substantially and as detailed above, but fails to disclose that said first region is adjacent to said second region ("adjacent" is interpreted as "in contact"). In other words, because the reference discloses a third region between and in contact with the first region and the second region, the third region prevents the first region from being in contact with the second region. However, the change would have been obvious to one of ordinary skill in the art at the time the invention was made ("the artisan"), because the artisan would easily recognize that even without the third region, the structure (and method thereof) would still be a diode, only that it would be much simpler to make (two layers instead of three layers).

Referring to **claims 4, 6, 14, 16, and 18**, the '154 patent discloses a diode and a method of fabricating thereof substantially and as detailed above, but fails to disclose a third or a fourth region, where the third or the fourth region is intrinsic. However, the artisan, at the time the invention was made, would easily recognize, therefore would have been obvious, that a diode

having an intrinsic region as claimed would increase the breakdown voltage, as is known in the art and as disclosed, for example, by Nemoto PGPUB-DOCUMENT-NUMBER: 20010015445, paragraph [0003].

Allowable Subject Matter

8. Claims 9 and 19 and respective dependent claims 10 and 20, in so far as in compliance with the objection noted above, are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is an examiner's statement of reasons for the indication of allowable subject matter: The cited art, whether taken singularly or in combination, especially when all limitations are considered within the claimed specific combination, fails to teach or render obvious a diode and a method of fabricating thereof having all limitations as recited in claim 1/2/5/7/9 (claims 1, 2, 5, 7, and 9) or claim 11/12/15/17/19 characterized in the fifth region as recited in claim 9 and 19 respectively.

Conclusion

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tu-Tu Ho whose telephone number is (571) 272-1778. The examiner can normally be reached on 6:30 am - 5:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, DAVID NELMS can be reached on (571) 272-1787. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

TH

Tu-Tu Ho
April 26, 2005